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U.S. PATENT DOCUMENTS

EXAMINER		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
(initials)		6,035,320	3/7/00	Kiriaki et al.	708	819	
✓		5,777,910	7/7/98	Lu	364	724.2	
✓		5,535,150	7/9/96	Chiang	364	724.19	

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Group 2100

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT
		WO 46867	9/16/99	PCT			

OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)

(initials)		"An Adaptive Multiple Echo Canceller for Slowly Time Varying Echo Paths", Yip and Etter, IEEE Transactions on Communications, October 1990
✓		"Digital Signal Processing", Alan V. Oppenheim et al., pp. 155-163
✓		"A 100 MHz Output Rate Analog-to-Digital Interface for PRML Magnetic-Disk Read Channels in 1.2 um CMOS", Gregory T. Uehara and Paul R. Gray, ISSCC94/Session 17/Disk-Drive Electronics/Paper FA 17.3, 1994 IEEE International Solid-State Circuits Conference, pp. 280-281
✓		"72 Mb/s PRML Disk-Drive Chann l Chip with an Analog Sampled Data Signal Processor", Richard G. Yamasaki t al., ISSCC94/Session 17/Disk-Drive Electronics/Paper FA 17.2, 1994 IEEE International Solid State Circuits Conference, pp. 278-279

EXAMINER		DATE CONSIDERED 12/2004

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Sheet 1 of 2

Form #62

FORM PTO 1449 (modified)

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LIST OF REFERENCES CITED BY APPLICANT(S)
(Use several sheets if necessary)

ATTY DOCKET NO. 13200 - 00017 (MP0042)	APPLICATION NO. 09/678,728
APPLICANT YAT-TUNG LAM	
FILING DATE October 4, 2000	GROUP 2121

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT

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		"A Discrete-Time Analog Signal Processor for Disk Read Channels", Ramon Gomez et al., ISSCC93/Session 13/Hard Disk and Tape Drives/Paper FA 13.1, 1993 ISSCC Slide Supplem nt, pp. 162-163 and 279-280
		"A 50 MHz 70 mW 8-Tap Adaptive Equalizer / Viterbi Sequence Detector in 1.2 um CMOS", Gregory T. Uehara et al., 1994 IEEE Custom Integrated Circuits Conference, pp. 51-54

EXAMINER		DATE CONSIDERED	12/200

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